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| 09/255,856      | 02/23/1999  | TOMIO IWASAKI        | 501.39631X00        | 9089             |

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EXAMINER

SMOOT, STEPHEN W

ART UNIT PAPER NUMBER

2813

DATE MAILED: 07/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/255,856

Applicant(s)

IWASAKI ET AL.

Examiner

Stephen W. Smoot

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 18 March 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-6,9-20,22-25 and 27-37 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1,2,5,6 and 32 is/are allowed.
- 6) ☒ Claim(s) 3,4,9,10,16-20,22-25,27-31 and 33-37 is/are rejected.
- 7) ☒ Claim(s) 11-15 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 February 1999 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

## **DETAILED ACTION**

This Office action is in response to applicant's CPA filed on 18 March 2003. The applicants were notified in a prior Office action (see Paper No. 29) that the request for a CPA has been treated as an RCE. It is further noted that the three months suspension requested by applicants under 37 CFR 1.103 has expired as of 02 July 2003.

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's arguments filed on 18 September 2002, that were submitted after final rejection, satisfy the submission requirement under 37 CFR 1.114 (see MPEP 706.07(h), part II) and will be considered in this Office action.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 4, 9-10, 16-20, 22-25, 27-31, 33-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Schacham-Diamand et al.

Referring to Fig. 13 of Schacham-Diamand et al., an embodiment whereby copper is deposited in trench regions of a semiconductor structure (see column 8, lines 58-61) is disclosed with the following features:

- Two trenches (25, 26) are formed in a dielectric layer (24) that in turn has been formed over a silicon substrate (see column 5, lines 13-32 and column 8, lines 32-39, 61-62);
- Copper interconnects (33) in contact with a catalytic seed layer (18a) are formed in the trenches (25, 26) such that the catalytic seed layer (18a) is sandwiched between the copper interconnects (33) and the dielectric layer (24);

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- The catalytic seed layer (18a) can be comprised of platinum or rhodium (see column 7, lines 29-35 and column 11, lines 21-22, 48-49);
- The catalytic seed layer (18a) lines the trenches (25, 26) and, as a consequence, the catalytic seed layer (18a) is between the copper interconnects (33) and the underlying silicon substrate (not shown in Fig. 13, but is designated as 54 in Fig. 20);
- A diffusion barrier layer (17a) that can be comprised of titanium nitride, tantalum or tungsten (see column 6, lines 35-37, column 7, lines 26-28, and column 9, lines 16-17);
- The catalytic seed layer (18a) is in contact with the diffusion barrier layer (17a) (see column 9, lines 14-20 and column 6, lines 45-47); and
- The catalytic seed layer (18a) is sandwiched between the diffusion barrier layer (17a) and the copper interconnects (33).

These are all of the structural limitations set forth in claims 9-10, 16-20, 27, 30-31, 33-37 of the applicant's invention.

Regarding claim 4, Fig. 19 is an embodiment that is similar to the above embodiment of Schacham-Diamand et al. that additionally features the catalytic seed layer (18b) lining a via (i.e. a plug) (see column 9, line 52 to column 10, line 18). So, Schacham-Diamand et al. disclose all of the structural limitations of claim 4.

Regarding claims 22-25, 28-29, Schacham-Diamand et al. further disclose that additional levels of copper utilizing their catalytic seed layer, separated by dielectric layers (55), can be formed over the substrate (54) using plugs (51) to couple the metal

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lines (52) with the M1 level coupled directly to the substrate (see Fig. 20 and column 10, lines 26-33). So, Schacham-Diamand et al. also disclose all of the structural limitations of claims 22-25, 28-29.

Regarding the "prevention of voids due to electromigration" limitation in the above claims, this property is presumed to be inherent to the disclosure of Schacham-Diamand et al., per MPEP 2112.01, because their disclosed structures are essentially identical to the applicant's structure as claimed in claims 4, 9-10, 16-20, 22-25, 27-31, 33-37.

Regarding the various PVD, CVD, plating, etc. limitations in the above claims, it is noted that these are process limitations and the examination of product-by-process claims are based on the structure implied by the process limitations (see MPEP 2113). It is further noted that per MPEP 2113, the burden now shifts to the applicant to show an unobvious difference between the above rejection under 35 USC 102 (e) and applicant's claims 4, 9-10, 16-20, 22-25, 27-31, 33-37.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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5. Claims 3, 30, 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hussein et al. in view of the IBM Technical Disclosure Bulletin.

Referring to Fig. 3 and column 3, lines 1-13, Hussein et al. disclose the following limitations set forth in claims 3, 30, 36: a semiconductor substrate (1), a dielectric layer (3) with vias (4), a diffusion barrier (5) formed over the dielectric layer (3) also lines the via walls (20) and the via bottom surface (22), and interconnect layers (7, 30) that can be copper (see column 3, lines 50-53). Layer 7 is a liner layer that is applied to the barrier layer 5 (see column 3, lines 55-57) and therefore layers 5 and 7 "neighbor " each other. Also, the barrier layer (5) is between the dielectric layer (3) and the interconnect layers (7, 30). However, Hussein et al. do not disclose ruthenium (nor, alternatively, rhodium, iridium, osmium, or platinum) as a diffusion barrier material. The IBM Technical Disclosure Bulletin does teach that ruthenium (as well as rhenium, osmium, and iridium) is an exceptional barrier against the diffusion of copper (see first sentence of final paragraph).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of the IBM Technical Disclosure Bulletin with those of Hussein et al. and use ruthenium as a diffusion barrier material. Hussein et al. recognize that copper diffusion into silicon and, also into any surrounding dielectric material, can result in defective circuitry (see column 1, lines 55-57).

***Allowable Subject Matter***

6. Claims 1-2, 5-6, 32 are allowed.

7. Claims 11-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

- Claims 1-2, 32 are allowed because the prior art of record does not teach or suggest a copper film interconnect, with a multi-layered copper structure, that is in contact with a neighboring layer of rhodium, ruthenium, iridium, osmium, or platinum, in combination with the other claim limitations;
- Claims 5-6 are allowed because the prior art of record does not teach or suggest a copper film interconnect structure that includes a plug with ruthenium as the primary constituent element, in combination with the other claim limitations; and
- Claims 11-15 would be allowable because the prior art of record does not teach or suggest a platinum film interconnect structure adjacent to a neighboring film that includes a material selected from a group consisting of rhodium, ruthenium, iridium, and osmium, in combination with the other claim limitations.



***Response to Arguments***

9. Applicant's arguments filed 18 September 2002, regarding the above rejections to claims 3, 30, 36 under 35 U.S.C. 103(a), have been fully considered but they are not persuasive.

Regarding applicant's argument that there is no proper motivation to combine Hussein et al. and the IBM Technical Disclosure Bulletin (see Paper No. 26, paragraph bridging pages 9-10 and paragraph bridging pages 13-14), the motivation as set forth in the IBM Technical Disclosure Bulletin is their discovery that one metal selected from the group consisting of rhenium, ruthenium, osmium, and iridium is an excellent barrier against the diffusion of copper (see first sentence of final paragraph) combined with the recognition by Hussein et al. that barrier layers are typically used in conjunction with copper interconnects to prevent copper from diffusing into the underlying circuitry (see column 1, lines 55-60).

Regarding the applicant's argument concerning the diffusion of copper into silicon versus the diffusion of copper into silicon oxide and the challenge to point out the pertinent teachings of Hussein et al. (see Paper No. 26, pages 10-11, 13), the applicant is first directed to column 1, lines 12-21 where Hussein et al. explain that interconnects include metal lines that connect to active and passive devices that are formed in a substrate. The substrate is typically silicon. Hussein et al. then go on to state that known structures (implying the above active/passive devices) are not illustrated (see

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column 2, lines 58-67). Fig. 1 clearly shows that dielectric layer (3) is formed on semiconductor substrate (1) (also see column 3, lines 1-2). Hussein et al. then state that the barrier layer (5) keeps metal from diffusing into the underlying (implying silicon substrate) and adjacent dielectric layer (see column 3, lines 9-11). The applicant is also referred to MPEP section 2144.01 regarding the use of implicit disclosures for supporting 35 USC 103(a) rejections.

Regarding the applicant's argument that there are unobvious differences based on the claimed processes used to obtain the claimed product (see Paper No. 26, pages 11-12, 14), the examiner notes that a declaration containing the to be relied upon evidence has yet to be filed with the Office. If it can be shown that the information provided in the "Sketch" was known by the applicant at the time of the invention, it might be sufficient to overcome the prior art rejection to claim 3, since the IBM Technical Disclosure Bulletin does not teach or suggest forming ruthenium films by sputtering. However, the examiner notes that claims 30, 36 would remain rejected, since the PVD film in these claims can be the neighboring film or the copper film and Hussein et al. suggest a sputtered copper liner layer (7) (see column 3, lines 43-58).

### ***Conclusion***

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 703-305-0168. The examiner can normally be reached on M-F (8:00am to 4:30pm).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

SWS  
July 23, 2003

  
CARL WHITEHEAD, JR.  
SUPERVISORY PATENT EXAMINER  
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